Course code	Course Name	L-T-P -Credits	Year of Introduction
EE462	Design of Digital Control Systems	3-0-0-3	2016

Prerequisite: Nil

Course Objectives

- To introduce the need and concept of digital control system.
- To impart knowledge about different strategies adopted in the design of digital controllers.
- To familiarize with the design of different types of digital controllers.

Syllabus

Basic digital control system-Pulse transfer function-Digital PID controller design- compensator design using frequency response - compensator design using root locus - Direct design-method of Ragazzini - Dead-beat controller design - State space analysis and controller design.

Expected outcome.

On successful completion, the students will have the ability to

i. design digital controllers.
ii. analyse discrete time system using state space methods.
iii. analyse the stability of discrete time system.

Text Books:

1. Benjamin C. Kuo, Digital Control Systems, 2/e, Saunders College Publishing, Philadelphia, 1992.
2. C. L. Philips, H. T. Nagle, Digital Control Systems, Prentice-Hall, Englewood Cliffs, New Jersey, 1995.
3. M. Gopal, Digital Control and State Variable Methods, Tata McGraw-Hill, 1997
4. Ogata K., Discrete-Time Control Systems, Pearson Education, Asia.

References:

1. Constantine H. Houpis and Gary B. Lamont, Digital Control Systems Theory, Hardware Software, McGraw Hill Book Company, 1985.
2. Isermann R., Digital Control Systems, Fundamentals, Deterministic Control, V. I, 2/e, Springer Verlag, 1989.
3. Liegh J. R., Applied Digital Control, Rinchart & Winston Inc., New Delhi.

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Basic digital control system- Examples - mathematical model-ZOH and FOH- choice of sampling rate-principles of discretization - Mapping between s-domain and z-domain	7	15%
II	Pulse transfer function- Different configurations for the design- Modified z-transform-Time responses of discrete data systems-Steady state performance.	7	15%
	FIRST INTERNAL EXAMINATION		
III	Digital PID and Compensator Design: Design of digital PID controller, Design of lag, lead compensators - based on frequency response method.	7	15%
IV	Digital Controller Design: Design based on root locus in the z-plane, direct design - method of Ragazzini. Dead-beat response design- Deadbeat controller.	7	15%
	SECOND INTERNAL EXAMINATION		
V	State variable model of discrete data systems -Various canonical form representations-controllable, observable, diagonal and Jordan forms-Conversion from state space to transfer function -Computation of state transition matrix using Cayley-Hamilton theorem and z-transform method	7	20%

VI	Digital state feedback controller design: Complete state and output Controllability, Observability, stabilizability and reachability - Loss of controllability and observability due to sampling.Pole placement design using state feedback for SISO systems.	7	20%
END SEMESTER EXAM			

QUESTION PAPER PATTERN:

Maximum Marks: 100 Exam Duration: 3Hourrs.

Part A: 8 compulsory questions.

One question from each module of Modules I - IV; and two each from Module V & VI.

Student has to answer all questions. (8 x5)=40

Part B: 3 questions uniformly covering Modules I & II. Student has to answer any 2 from the 3 questions: (2 x 10) =20. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Part C: 3 questions uniformly covering Modules III & IV. Student has to answer any 2 from the 3 questions: (2 x 10) =20. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Part D: 3 questions uniformly covering Modules V & VI. Student has to answer any 2 from the 3 questions: (2 x 10) =20. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.